What Is Claimed Is:

1. A delay optimization designing system for a logic circuit including a plurality of flip-flops and a combinational circuit formed from logic circuit elements, comprising:

flip-flop selection means for selecting any flip-flop not to be substituted into a latch from within a given logic circuit;

flip-flop searching means for searching any flip-flop having a delay margin from among the flip-flops which are not selected by said flip-flop selection means; and

latch substitution means for substituting any flip-flop searched by said flip-flop searching means into a latch which passes a signal to the output side therethrough faster than the searched flip-flop.

2. A delay optimization designing system for a logic circuit as claimed in claim 1, wherein the flip-flop holds data inputted in response to an edge of a clock upon variation from a first level to a second level, and the latch substituted by said latch substitution means passes input data when the clock indicates the first level therethrough to the output side.

3. A delay optimization designing system for a logic circuit as claimed in claim 1, further comprising latch

insertion means for inserting a second latch, which passes input data at a timing different from that of the latch substituted by said latch substitution means, into a predetermined portion of the logic circuit.

4. A delay optimization designing system for a logic circuit as claimed in claim 3, wherein the second latch inserted by said latch insertion means passes input data when the clock indicates the second level therethrough to the output side.

5. A delay optimization designing system for a logic circuit as claimed in claim 3, wherein the second latch inserted by said latch insertion means is arranged on the output side of the latch substituted by said latch substitution means.

6. A delay optimization designing method for a logic circuit including a plurality of flip-flops and a combinational circuit formed from logic circuit elements, comprising:

a flip-flop selection step of selecting any flip-flop not to be substituted into a latch from within a given logic circuit;

a flip-flop searching step of searching any flip-flop having a delay margin from among the flip-flops which are not selected at the flip-flop selection step; and

a latch substitution step of substituting any flip-flop searched at the flip-flop searching step into a latch which passes a signal to the output side therethrough faster than the searched flip-flop.

7. A delay optimization designing method for a logic circuit as claimed in claim 6, wherein the flip-flop holds data inputted in response to an edge of a clock upon variation from a first level to a second level, and the latch substituted at the latch substitution step passes input data when the clock indicates the first level therethrough to the output side.

8. A delay optimization designing method for a logic circuit as claimed in claim 6, further comprising a latch insertion step of inserting a second latch, which passes input data at a timing different from that of the latch substituted at the latch substitution step, into a predetermined portion of the logic circuit.

9. A delay optimization designing method for a logic circuit as claimed in claim 8, wherein the second latch inserted at the latch insertion step passes input data when the clock indicates the second level therethrough to the output side.

10. A delay optimization designing method for a logic circuit as claimed in claim 8, wherein the second latch

inserted at the latch insertion step is arranged on the output side of the latch substituted at the latch substitution step.

11. A program for causing a computer to perform a delay optimization designing method for a logic circuit including a plurality of flip-flops and a combinational circuit formed from logic circuit elements, comprising:

a flip-flop selection step of selecting any flip-flop not to be substituted into a latch from within a given logic circuit;

a flip-flop searching step of searching any flip-flop having a delay margin from among the flip-flops which are not selected at the flip-flop selection step; and

a latch substitution step of substituting any flip-flop searched at the flip-flop searching step into a latch which passes a signal to the output side therethrough faster than the searched flip-flop.

12. A program as claimed in claim 11, wherein the flip-flop holds data inputted in response to an edge of a clock upon variation from a first level to a second level, and the latch substituted at the latch substitution step passes input data when the clock indicates the first level therethrough to the output side.

13. A program as claimed in claim 11, further comprising a

latch insertion step of inserting a second latch, which passes input data at a timing different from that of the latch substituted at the latch substitution step, into a predetermined portion of the logic circuit.

14. A program as claimed in claim 13, wherein the second latch inserted at the latch insertion step passes input data when the clock indicates the second level therethrough to the output side.

15. A program as claimed in claim 13, wherein the second latch inserted at the latch insertion step is arranged on the output side of the latch substituted at the latch substitution step.